

Docket Number RA-5548
Examiner Russell Guill, GUA 2123

Office Action Response
September 24, 2007

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Please Amend the Specification as Follows:

Please amend the Abstract as follows:

"An apparatus and method for generating test files for design verification of a simulated integrated circuit design such as a cache memory circuit, that ~~includes~~ involve steps of creating a series of functions, updating a data integrity buffer after each function is created, creating a series of integrity check functions from the data in the data integrity buffer, and writing the series of functions and the series of integrity check functions to a test file. This file can be compiled if necessary and executed by a software or hardware simulator."